Changes In SpRC-V5 relative to SRC-V4

1) AVDD lines should have one 100nF type 0402 capacitor near SVX4 pin 2 or 15 and one 0402 capacitor 2.2 uF (Digikey 490-4518-1-ND) near connector.
2) The one of the internal layers should have large AGND area. The signals from the strips are all referenced to AGND, therefore this part of PCB should be surrounded by AGND.
3) The copper under the SVX4 should be AGND, not GND!
4) All control signals (Bus[7:0], clocks, ChMode, BEMode, FEMode, CalSR, L1, PRD2, PRD1, PARst etc..) are all referenced to DGND, therefore the DGND should surround these signals on the PCB.
5) The DGND should have its own return path, connected to DGND pin of the connector and connected to the AGND at one point per board via a zero ohm resistor 0603 type.
6) Do not put resistor 100 Ohm between PRIIN+ and PRIIn- lines of SVX4. This resistors will be placed on the motherboard
7) The terminating resistors R23:R36 also should be not on the SpRC but placed on the motherboard.
8) Both ADC_HVBias lines and all related components (R15, R16, R18, R25, U7) are not necessary. The limiting resistor R14 1.0M and filtering capacitor C143 22nF type 0805 (445-2281-1-ND) should stay.
9) We will not use U5 and U6 in normal condition but it is convenient to have the pads for them on the board for testing and modifications.
10) The board should have 2 connectors.
P1 – for LVDS signals: Bus[7:0], OBDV, PriIn, PriOut, FEClk, BEClk. Total 13 pairs.
P2 – for the single-ended signals and power. ChMode, BEMode, FEMode, CalSR, L1, PRD2, PRD1, PARst. Total 8 signals plus DVDD, AVDD, AGND, DGND
11) The USESEU pin of the should be connected to DVDD, not GND, therefore the pad on the left side of the SVX4 between D0Mode and ISLOPE should be DVDD, not GND.